rejections under 35 U.S.C. §112, and under 35 U.S.C. §102(e) as anticipated by Jain (U.S. Patent No. 5,821,168), have been withdrawn.

Claims 1-16 and 26 are pending after entry of this Amendment. Claims 1, 2, 6, 7, 10, 13, and 14 are herein amended to clarify the present invention. The amendments include further clarifying the low dielectric constant layer, also previously claimed as a low dielectric constant layer to define a trench dielectric layer over the inorganic dielectric layer, as a carbon doped oxide layer. Further, the carbon doped oxide layer is claimed to have a dielectric constant of about 3.0 or less. The Examiner is directed to, for example, page 11, lines 6-16, of the specification as originally filed for support of the present amendments. Applicants respectfully submit no new matter is claimed or introduced.

Rejections under 35 U.S.C. §102

Claims 1-5, 10-14 and 26 were rejected under 35 U.S.C. §102(e) as being anticipated by Smith (U.S. Patent No. 6,277,733). Applicants traverse this rejection and request reconsideration.

Smith teaches an electronic device and methods for fabricating the same on a semiconductor wafer. While Smith teaches a plurality of layers to the disclosed device, of particular relevance to the presently claimed invention is a via layer, identified in the Smith reference as 424, and a trench layer, identified in the Smith reference as 430. As noted in the Smith reference at col. 3, lines 26-28, "dielectric layer 424 (preferably comprised of FSG, BPSG, PSG, TEOS, aerogel, xerogel, HSQ or any other low dielectric constant material)" is a low dielectric constant layer. The reference states at col. 3, lines 55-59, that "dielectric layer 430 is comprised of TEOS, FSG, PBSG, PSG, HSQ, or a low dielectric constant material, such as aerogel, xerogel, or a polymer (such as fluorinated parylene)." Dielectric layer 430 therefore can be fabricated of the named materials, or a polymer. Smith, therefore, teaches a trench layer which can be of a number of materials including a low dielectric constant material, over a via layer of a low dielectric constant material.

The present invention claims, as amended herein, a carbon doped oxide trench layer over an inorganic dielectric (a silicon dioxide layer in independent claim 10) via layer. The reference teaches a low dielectric constant (among other materials) trench layer over a low dielectric constant via layer. The reference does not teach a carbon

doped oxide trench layer, and therefore does not teach each and every feature of Applicants' independent claims 1 and 10. Applicants respectfully request that the §102 rejection be withdrawn. The dependent claims, depending directly or indirectly from independent claims 1 and 10, are submitted to be patentable over the cited reference for at least the same reasons.

Claims 1-4 and 10-16 were rejected under 35 U.S.C. §102(e) as being anticipated by Wang et al. (U.S. Patent No. 6,255,735, hereinafter Wang '735). Applicants traverse this rejection and request reconsideration.

Wang '735 teach a structure similar to Smith which includes a low k dielectric trench layer over a low k dielectric via layer. Wang '735 does not teach a carbon doped oxide trench layer over an inorganic dielectric via layer. Wang '735 therefore does not teach each and every feature of the claimed invention as recited in amended independent claims 1 and 10. Dependent claims 2-4 and 11-16, depending directly or indirectly from independent claims 1 and 10, are submitted to be patentable over the cited reference for at least the same reasons. Applicants respectfully request this rejection be withdrawn.

Claims 1-4 and 10-16 were rejected under 35 U.S.C. §102(e) as being anticipated by Wang et al. (U.S. Patent No. 6,207,577, hereinafter Wang '577). Applicants traverse this rejection and request reconsideration.

Wang '577 teaches a similar structure to Wang '735, in that Wang '577 teaches a low dielectric constant trench layer over an oxide via layer. Wang '577 does not teach a carbon doped oxide trench layer over an inorganic dielectric via layer. Wang '577, therefore, does not teach each and every feature of Applicants' claimed invention as recited in amended independent claims 1 and 10, as well as in the dependent claims therefrom, and Applicants request the §102 rejection be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 4-9, 15-16, and 26 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jain, Smith, Wang '735, and Wang '577 as applied to claims 1 or 10 above, in further view of Usami (U.S. Patent No. 6,077,574). Applicants respectfully traverse this rejection and request reconsideration.

Dependent claims 4-9, 15-16, and 26 were rejected under §103 with independent claims 1 and 10 rejected as discussed above. To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, at the time of

invention, to modify the reference or to combine reference teaching. Additionally, there must be a reasonable expectation of success, and the combination of prior art references must teach or suggest all of the claim limitations. Applicant respectfully submits that the Office has failed to establish a *prima facie* case of obviousness.

Applicants' amended independent claims recite the trench layer as a carbon doped oxide layer. On page 10 of the Final Office Action, it is asserted that "Usami teach depositing a carbon-doped oxide layer for forming a low dielectric constant layer with a good resistance to moisture and resistance to heat. It would have been obvious for those skilled in the art to combine the teaching of Usami to the process of either Jain, Smith, Wang '577, or Wang '735 to deposit the carbon-doped oxide layer as the low dielectric constant layer for defining the trench for interconnection in a device with low RC, good resistance to moisture and resistance to heat." Applicants respectfully submit the Examiner has mischaracterized the Usami reference, and even if the references were combined as suggested, the combined references fail to teach or suggest all the claim limitations.

Usami teaches a fluorine ***and*** carbon doped silicon oxide dielectric film. As is well known, the properties of a fluorine ***and*** carbon doped dielectric are fundamentally different than a carbon doped oxide layer as claimed by Applicants. While the properties asserted by the Examiner may be desirable in some applications, Applicants are claiming a carbon doped oxide layer. Nothing in the Usami reference teaches or suggests a desirability for a carbon doped oxide layer, and even suggests that carbon concentrations without fluorine are *un*desirable (see col. 3, lines 11-19). In this regard, Usami *teaches away* from the present invention.

Applicants respectfully submit that the asserted combination fails to teach or suggest all claim limitations of the present invention. Further, the Usami reference teaches away from the Applicants claimed invention. Therefore, the Office has failed to establish a *prima facie* case of obviousness. Applicants submit that claims 4-9, 15-16, and 26 as amended herein are patentable over the cited combinations under 35 U.S.C. §103(a), as are independent claims 1 and 10 as amended herein. Applicants therefore request the §103 rejections be withdrawn.

In view of the foregoing, Applicants respectfully request reconsideration of claims 1-16 and 26, and submit that these claims are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested. If Examiner has any

questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6900, ext. 6905. If any additional fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM1P106A). A copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE & PENILLA, L.L.P.

Rick von Wohld, Esq.
Reg. No. 48,018

MARTINE & PENILLA, LLP
710 Lakeway Drive, Suite 170
Sunnyvale, California 94085
Customer Number 25920

MARKED UP CLAIMS

1. (Twice Amended) A method for making a dielectric structure for dual-damascene applications, the method comprising:

providing a substrate;

fabricating metallization lines within the substrate;

forming a barrier layer over the metallization lines and the substrate;

forming an inorganic dielectric layer to define a via dielectric layer over the barrier layer, the inorganic dielectric layer being highly selective relative to the barrier layer when etched; and

forming a [low dielectric constant] carbon doped oxide layer to define a trench dielectric layer over the inorganic dielectric layer.

2. (Amended) A method for making a dielectric structure for dual-damascene applications as recited in claim 1, further comprising:

forming a trench in the [low dielectric constant] carbon doped oxide layer using a first etch chemistry.

6. (Amended) A method for making a dielectric structure for dual-damascene applications as recited in claim 5, wherein the [forming of the low dielectric constant layer includes,

depositing a carbon doped oxide] carbon doped oxide layer is a low dielectric constant layer having a dielectric constant of about and no greater than 3.0.

7. (Amended) A method for making a dielectric structure for dual-damascene applications as recited in claim 3, wherein the inorganic dielectric layer is one

of a TEOS oxide layer and a fluorine doped oxide layer[, and the low dielectric constant layer is a carbon doped oxide layer].

10. (Twice Amended) A method for making a multi-layer inter-metal dielectric over a substrate, comprising:

forming a barrier layer over the substrate;

forming a silicon dioxide layer over the barrier layer;

forming a [low dielectric constant] carbon doped oxide layer over the silicon dioxide layer;

forming a trench through the [low dielectric constant] carbon doped oxide layer; and

forming a via in the trench extending through the silicon dioxide layer to the barrier layer.

13. (Amended) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 12, wherein the [forming of the low dielectric constant layer, includes,

depositing one of a carbon doped oxide layer and an organic dielectric layer] carbon doped oxide layer is a low dielectric constant layer having a dielectric constant less than or equal to about 3.0.

14. (Twice Amended) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 10, wherein forming the via in the trench extending to the barrier layer further includes,

implementing a first chemistry optimized to etch through the [low dielectric constant] carbon doped oxide layer; and

implementing a second chemistry which is different than the first etch chemistry and is optimized to etch through the silicon dioxide layer.